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| **Course Name:** | **Electronic Circuits Analysis and Design** | **Semester:** | **IV** |
| **Date of Performance:** | **25-01-2021** | **Batch No:** | **B2** |
| **Faculty Name:** | **Prof. Sonia** | **Roll No:** | **1912052** |
| **Faculty Sign & Date:** |  | **Grade/Marks:** | **/25** |

**Experiment No: 1**

**Title: To study the frequency response of a FET amplifier.**

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| **Aim and Objective of the Experiment:** To study the frequency response of a FET amplifier.  1) Bypass  2) Un bypass |
| 1) To calculate maximum gain.  2) To calculate lower cut off frequency, higher cut off frequency and bandwidth from frequency response. |

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| **COs to be achieved:** |
| CO1: Learn the dependency of the amplifier gain over the frequency range |

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| **Theory:** |
| The analysis of low-frequency response and high frequency response of a FET amplifier is similar as that of a BJT amplifier. For a single stage FET amplifier, the high frequency characteristic of the amplifier is determined by the inter electrode and wiring capacitances. The gate-to-source capacitor (Cgs) and the gate-to-drain (Cgd) capacitance typically vary from 1-10 pF, while the capacitance (Cds) is usually quite a bit smaller ranging from 0.1-1 pF. At high frequency miller capacitance will approach a short-circuit equivalent and Vgs will drop and in value and reduce the overall gain. |

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| **Circuit Diagram:** |
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| **Stepwise-Procedure:** |
| 1. Make the connections as per the Circuit diagram.  2. Apply the sinusoidal input signal to the circuit.  3 Observe transient response of the circuit  4. Apply AC signal at the input of the circuit  5. Observe the Frequency response of the circuit  6. Calculate maximum gain and lower cut off frequency, higher cut off frequency bandwidth theoretically and practically. |

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| **Observation Table:** |
| **A)Bypass**  **1) Transient response**   |  |  |  |  | | --- | --- | --- | --- | | **Sr No** | **Input Signal** | **Vo(Thr)** | **Vo(Prac)** | | **1.** | **20 mV (p-p)** | **92.3199 mV** | **88.24625 mV** |   **2) Frequency Response**   |  |  |  | | --- | --- | --- | | **Sr No** | **Input Signal frequency** | **Highest Gain in dB** | | **1** | **100HZ** | **32.036159dB** | | **2** | **1KHz** | **36.141194dB** | | **3** | **10KHz** | **36.821681dB** | | **4** | **100KHz** | **36.867439dB** | | **5** | **1MHz** | **36.597093dB** | | **6** | **10MHz** | **33.531187dB** |     **3) fL, fH, Bandwidth**  BW=8.99MHz  FL=230.409Hz  FH=8.9984MHz  **B)Unbypass**  **1) Transient response**   |  |  |  |  | | --- | --- | --- | --- | | **Sr No** | **Input Signal** | **Vo(Thr)** | **Vo(Prac)** | | **1** | **20 mV (p-p)** | **22.625 mV** | **22.581499 mV** |   **2) Frequency Response**   |  |  |  | | --- | --- | --- | | **Sr No** | **Input Signal frequency** | **Highest Gain in dB** | | **1** | **100Hz** | **34.122517dB** | | **2** | **1KHz** | **35.794062dB** | | **3** | **10KHz** | **35.955868dB** | | **4** | **100KHz** | **35.940888dB** | | **5** | **1MHz** | **35.653102dB** | | **6** | **10MHz** | **32.57915dB** |     **3) fL, fH, Bandwidth**  BW= 8.8MHz  FL=59.56621Hz  FH=8.8104MHz |

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| **Calculation:** |
| **A.C. Analysis:** |

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| **Waveform** |
| **Unbypassed**    **Bypassed** |

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| **Post Lab Subjective/Objective type Questions:** |
| 1. What are the causes of roll off in gain in FET amplifier? 2. Why gain of FET amplifier falls at higher frequencies?   The low input impedance offered by the capacitor {C} present in the circuit and also the **transistor gain reduces the output at high frequency** are the reason off gain falling down at high frequencies.   1. Is there any difference between the frequency responses of a BJT amplifier than FET amplifier? If so, Why? |

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| **Conclusion:** |
| * In this experiment, we measured the mid-band voltage and the bandwidth of single stage JFET amplifier circuit. |

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| **Signature of faculty in-charge with Date:** |